EE842

Eighth Semester B.E. Degree Examination, Dec 08 / Jan 09
VLSI Circuits and Design

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. With the help of cross sectional view and typical processing steps, explain the n – well CMOS fabrication process. **(12 Marks)**

b. Briefly discuss the comparison between the CMOS and Bipolar technologies. **(08 Marks)**

2 a. Discuss the aspects of MOS Transistor threshold voltage with relevant equation. **(06 Marks)**

b. An inverter (nMOS) is driven directly by another inverter. Show that $\frac{Z_{pu}}{Z_{pd}} = \frac{4}{1}$. **(06 Marks)**

c. With a neat diagram, explain the Latch-up in CMOS circuits. **(08 Marks)**

3 a. With neat diagram, explain the design rules for wires, transistor design rules and contacts. **(10 Marks)**

b. Draw the stick diagram of inverter with respect to i) nMOS ii) CMOS iii) BiCMOS. **(10 Marks)**

4 a. For the circuit shown in figure 4(a), show that the transit time τ_{sd} and the delay time τ are interchangeable. **(08 Marks)**

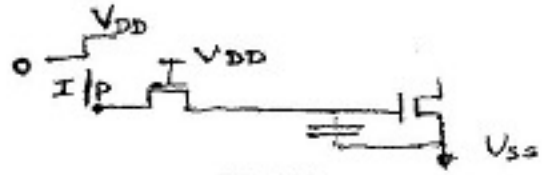

Fig.4(a)

b. Explain the working of a inverting type nMOS super buffer. **(06 Marks)**

c. In brief, explain the various components which contribute to the overall wiring capacitance. **(06 Marks)**

5 a. Calculate the effects of scaling on the following parameters.

i) Gate delay T_d.
ii) Channel resistance R_{ON}.
iii) Current density J.
iv) Switching energy per gate E_g.
v) Power - speed product P_T.

(10 Marks)

b. Compare the propagation delay of metal interconnect and optical interconnect by calculating the numerical value in both interconnects. **(10 Marks)**

6 a. Obtain the MOS diagram and slide diagram of a 2 input NOR gate with respect to i) nMOS ii) CMOS. **(07 Marks)**

b. Explain the structural design of parity generator and hence derive one – bit basic cell. **(07 Marks)**

c. Draw the logic arrangement of 4-line gray code to binary code converter and obtain one possible arrangement for an exclusive OR – gate. **(06 Marks)**

7 a. Design a 4 - bit shifter using i) cross bar switch ii) Barrel – type. **(10 Marks)**

b. Explain the design process of 4 – bit adder and obtain the multiplexer based adder logic arrangement. **(10 Marks)**

8 Write short notes on:

a. Alternate forms of pullup
b. MOS design styles
c. Scaling models.
d. Switch logic. **(20 Marks)**

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